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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/807,311	03/24/2004	Atsushi Yoshimura	04329.3292	3790

22852 7590 06/13/2005

FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER LLP
901 NEW YORK AVENUE, NW
WASHINGTON, DC 20001-4413

EXAMINER	
DIAZ, JOSE R	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 06/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/807,311	YOSHIMURA, ATSUSHI	
	Examiner	Art Unit	
	José R. Díaz	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *1-8,17 and 18* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9-16,19 and 20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/24/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 9-11, 13 and 15-16 are rejected under 35 U.S.C. 102(e) as being anticipated by Isaak (US Pat. No. 6,472,735 B2).

Regarding claim 9, Isaak teaches a semiconductor device comprising:

a first substrate (1st substrate 14) including an integrated circuit chip (1st chip 72) [See figure 2, attached below], first connection terminals (Terminals 82) electrically connected to terminals of the integrated circuit chip (24) [see fig. 2], and a first connection portion (consider through hole 32 formed in 1st substrate 14) spaced from the first connection terminals (Terminals 82) [see fig. 2];

a second substrate (2nd substrate) stacked on the first substrate [see fig. 2, attached below] and including second connection terminals (please consider terminals 51) and a second connection portion (consider 2nd connection portion formed in the 2nd substrate as shown in figure 3, attached below) spaced from the second connection terminals (51) [consider the space S_1 which is formed between the bottom surface of the 2nd connection portion and the upper surface of the second connection 51 shown in fig. 3, attached below]; and

a metal material portion (26) provided between the first connection portion and the second connection portion (fig. 2) and bonding the first connection portion to the second connection portion [please note that portions 30 and 44 of metal 26 are shown bonded with an epoxy component (49 and 50) in figure 3, attached below].

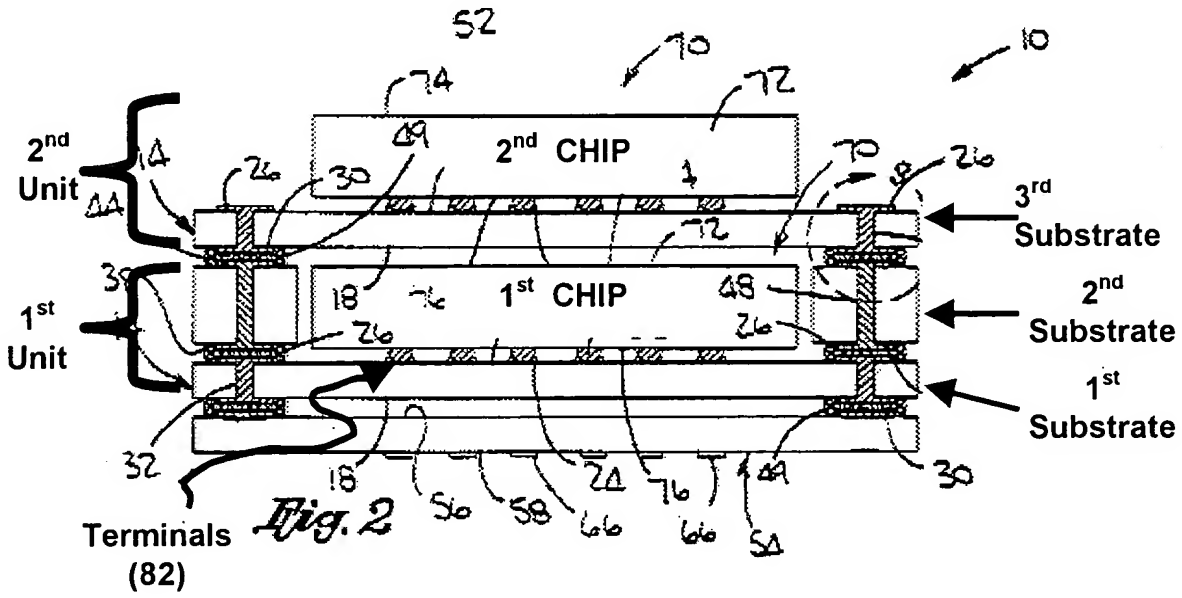


Fig. 2

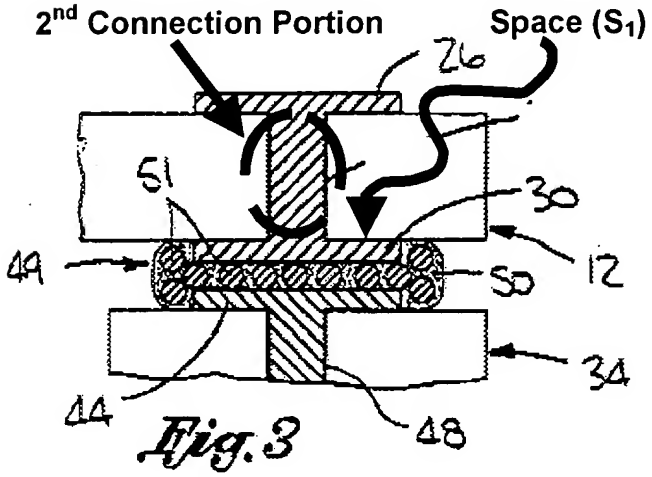


Fig. 3

Regarding claim 10, Isaak further teaches a plurality of unit substrates (1st Unit and 2nd Unit as shown in fig. 2, attached above) that are stacked, each of the unit substrates being formed of the first (14) and second (34) substrates stacked (see fig. 2. and col. 8, lines 2-3. Please note that although it is not shown in the figures, Isaak, in col. 8, ll. 2-3, further teaches that an additional second substrate 34 can be provided on the 3rd substrate].

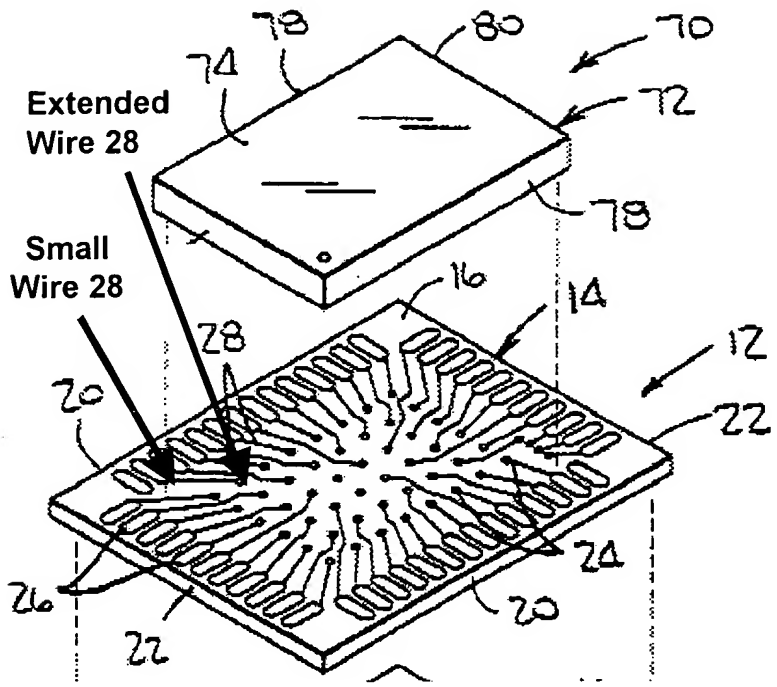
Regarding claim 11, Isaak further teaches an adhesive sheet (49,50) interposed between the unit substrates (1st Unit and 2nd Unit) adjacent each other a stacking direction and bonding the unit substrates together (see figs. 2 and 3, attached above).

Regarding claim 13, Isaak further teaches that the first connection portion is a first dummy pad (30) provided on the first substrate (14) [see fig. 3], and the second connection portion is a second dummy pad (44) provided on the second substrate (34) [see fig. 3]. [1]

Regarding claim 15, Isaak further teaches that the metal material portion (26) is formed of solder, tin, or an Sn-Bi alloy [col. 7, lines 58-61 and col. 8, lines 26-30].

Regarding claim 16, Isaak further teaches that the adhesive sheet (49, 50) is formed of resin [consider the epoxy material as disclosed in col. 61-63].

[1] Please note that the examiner considered the term "dummy" as merely a label, which was given by applicant to the structure of the instance device and does not distinguish over the structure taught by Isaak.



3. Claims 9-12 and 16 are rejected under 35 U.S.C. 102(e) as being anticipated by Imoto (JP 2001-068624).

Regarding claim 9, Imoto teaches a semiconductor device comprising:

a first substrate (1 and 50) including an integrated circuit chip (5) [See figures 4 and 8], first connection terminals (7 and 31b) electrically connected to terminals of the integrated circuit chip (11) [see figs. 3 and 8], and a first connection portion (31a) spaced from the first connection terminals (7) [See fig. 8];

a second substrate (20 and 40) stacked on the first substrate [see figs. 4 and 8] and including second connection terminals (2 and 31b) [see figs. 4 and 8] and a second connection portion (31a) spaced from the second connection terminals (2 and 31b) [See fig. 8]; and

a metal material portion (please note that via 31a also includes conductive 2 and 7, as show in figures 4) provided between the first connection portion and the second connection portion (fig. 8) and bonding the first connection portion to the second connection portion [see fig. 8].

Regarding claim 10, Imoto further teaches a plurality of unit substrates (each comprises of substrates 40 and 50) that are stacked, each of the unit substrates being formed of the first (50) and second (40) substrates stacked [see fig. 8].

Regarding claims 11 and 16, Imoto further teaches an adhesive sheet (4) made of a resin material interposed between the unit substrates adjacent each other a stacking direction and bonding the unit substrates together (see fig. 4 and paragraph [0015] of translation).

Regarding claim 12, Imoto further teaches that the first connection portion is a first dummy terminal provided between the first connection terminals adjacent to each other in a plane direction, and the second connection portion is a second dummy terminal provided between the second connection terminals adjacent to each other in the plane direction [consider the terminal 31a connected to ground as the dummy terminal. See fig. 8]. [2]

4. Claims 19-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Glenn et al. (US Pat. No. 6,577,013 B1).

Regarding claim 19, Glenn et al. teaches a semiconductor device comprising:

[2] Please note that the examiner considered the term "dummy" as merely a label, which was given by applicant to the structure of the instance device and does not distinguish over the structure taught by Imoto.

a plurality of unit substrates each comprising a first substrate (16) and a second substrate (64) stacked [see fig. 10], the first substrate (16) including an integrated circuit chip (18) [see fig. 10] and first connection terminals electrically (22) connected to terminals of the integrated circuit chip (24) [see fig. 4, col. 3, lines 66-67 and col. 4, lines 1-3], the second substrate (62) including second connection terminals (42) electrically connected to the first connection terminals (22) [see fig. 10]; and

an adhesive sheet (66) interposed between the unit substrates adjacent to each other a stacking direction (consider the adhesive sheet (66) positioned on top of layer 62) and bonding the unit substrates together [see figs. 10-11].

Regarding claim 20, Glenn et al. further teaches that the adhesive sheet (66) is formed of resin [col. 9, lines 4-5, 15-17 and 27-28].

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was

not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Imoto (JP 2001-068624) in view of Glenn et al. (US Pat. No. 6,577,013 B1).

Regarding claim 14, Imoto fails to teach that the first connection portion is a first alignment mark provided on the first substrate and used to align the first substrate with the second substrate, and the second connection portion is a second alignment mark provided on the second substrate and used to align the first substrate with the second substrate.

However, Glenn et al. teaches a package comprising first and second substrates (16 and 62) [see fig. 10], holes (32) formed in substrate (16) [see fig. 4], holes (68) formed in substrate (62) [see fig. 10], and pins (42) [see figs. 10]. Please note that pins (42) are inserted through holes (16 and 68) [see figs. 10], which inherently serve as an alignment mark to position the pins 42 accurately in the package [see figs. 10].

Imoto and Glenn et al. are analogous art because they are from the same field of endeavor as applicant's invention. At the time of the invention it would have been obvious to a person of ordinary skill in the art to bond the first and second substrate by using pins inserted through holes serving as alignment marks. The motivation for doing so, as is taught by Glenn et al., is reducing packing cost (col. 2, lines 4-5). Therefore, it would have been obvious to combine Glenn et al. with Imoto to obtain the invention of claim 14.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following references teach a stacked structure: Farnworth et al. (US Pat. No. 6,020,629), figure 2d; Eto et al. (US Pat. No. 6,774,478 B2), figure 2C; and Kasatani (US Pat. No. 6,617,695 B1), figure 8.

Correspondence

Any inquiry concerning this communication or earlier communications from the examiner should be directed to José R. Díaz whose telephone number is (571) 272-1727. The examiner can normally be reached on Monday through Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER

4/8/05

José R. Díaz
Examiner
Art Unit 2815